Journal of Engineering Research and Reports

14(4): 20-24, 2020; Article no.JERR.58632
ISSN: 2582-2926

Metallized Semiconductor Die for Long Wire Interconnect

Frederick Ray I. Gomez[1*] and Rennier S. Rodriguez[1]

[1]*New Product Development & Introduction, STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.*

Authors' contributions

This work was carried out in collaboration among the authors. Both authors read, reviewed, and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2020/v14i417131
Editor(s):
(1) Dr. David Armando Contreras-Solorio, University of Zacatecas, Mexico.
Reviewers:
(1) Reem Rafea Mohammed, University of Baghdad, Iraq.
(2) Josephine Ying Chyi Liew, Universiti Putra Malaysia, Malaysia.
Complete Peer review History: http://www.sdiarticle4.com/review-history/58632

Original Research Article

Received 06 May 2020
Accepted 11 July 2020
Published 24 July 2020

ABSTRACT

This paper focused on the integration of metallized silicon die in design layout of quad-flat no-leads package (QFN) and ball grid array (BGA) devices. The metallized silicon die is fabricated with a conductive top layer where the junction for wire interconnection is created. The conductive top layer formed an intermetallic connection between the gold or copper wire and aluminum metal on the conductive outer layer to produce electrical continuity in the device circuitry. Incorporating the design on conventional QFN and BGA eliminates long wiring layout in the system that is the primary cause of electrical shorting rejection during integrated circuit assembly and testing. For subsequent works, the design could be applied for packages with similar requirement and/or configuration.

Keywords: BGA; QFN; wirebond; package design.

1. INTRODUCTION

Nowadays, we experienced rapid advancement in our mobile, electronic wearables, computer, and laptop in terms of features and performance and still has a positive promise from electronic manufacturers to create improvement in the coming years. This is realized through multiple

**Corresponding author: Email: frederick-ray.gomez@st.com, f.i.gomez@ieee.org;*

innovations in the surface mount devices which is the core of every electronic devices. In the area of integrated circuit assembly, densification of integrated circuit (IC) device is achieved through incorporating multiple silicon die set-up or multiple stack-up configuration in the design layout of the device to increase the number of semiconductor die on a single IC unit. With multiple semiconductor die structure, there will be more transistors, resistors and active components that can function in a single unit to create an increased in the performance of the device.

The introduction of densified version of quad-flat no-leads (QFN) and ball grid array (BGA) package however comes with multiple assembly challenges. Densification offers many challenges for IC devices due to the existing constraint in equipment, manufacturability and design aspect [1-5]. The increase in numbers of active components inside the semiconductor die creates adjustments in the bond pad opening (BPO) and bond pad pitch (BPP) requirement and increased input/output (I/O) count. With the required smaller BPO and closer pitching of the bond pad, the required wire became smaller in diameter that needs to be connected to a required I/O location. Smaller diameter of wire easily collapses when it is hit by the mold fillers during the encapsulation process forcing it to be electrically shorted with the neighboring wire. This scenario is frequently observed on longest wire layout (700 microns length).

In this paper, a new layout design is discussed and presented. The innovation is consisting of a metallized silicon die that will be incorporated in the layout. The conventional wiring technique of 1-step connection is replaced by a 2-step wiring with a metallized silicon die be the junction between the connection. In this case, the wiring can be re-positioned to a more secure and stable state away from possibility of wire shorting. Implementing this design on conventional QFN and BGA eliminates assembly rejection related to fine and complex wiring layout such as sag wire, shorted wire, etc.

2. PACKAGE AND PROCESS DESIGN SOLUTION

Resolving the wire shorting on the longest wire connection as shown in Fig. 1A is the objective of the design. The package design shows a wire span of greater than 700 microns extending from the die to the I/O terminal. The said layout is highlighted with wire shorting and wire sway greater than the specification requirement. The wire shorting is observed between wire a and b where wire a became electrically shorted to wire b. There is a measured shift in the wire span of wire a while there is no measured shifting in the position of wire b. The wire sway located in group c and the measured shift in the placement is greater than the required 10% from the required specification limit. The improvement and design solution is presented in Fig. 1B wherein a metallized silicon die is incorporated in the affected wire location. The 1st segment of the wire will be bonded from the silicon die to the conductive layer (top portion of the metallized die) then the 2nd segment will connect the metallized silicon die to the I/O terminal.

A clear illustration of package 3D computer-aided design (CAD) modeling is shown if Fig. 2. The 1st segment of wire connects the silicon die to the metallized die and then the 2nd segment of wiring is repositioned with distance from the neighboring wire. In addition, it is known from the assembly experience that a shorter wire structure is more robust than longer wiring. In this case, the 2 segments of wiring are more stable during assembly mainly because of shorter span thus less wire sway. Moreover, maximum and minimum wire lengths for specific wire sizes are defined by assembly design rules document [4].

The configuration of the metallized die is explained in Fig. 3. The connection of the 1st and 2nd wiring is established from the 1st layer of conductive pads. Conductive pad can be fabricated using different metal configuration such as aluminized wafer or metal deposited wafer. The aluminized wafer has an aluminum metal deposited on the outer layer (top portion) where in can produce intermetallic and electrical continuity to the semiconductor wire. A nickel-palladium-gold (NiPdAu) wafer can be an alternative for the conductive pads, though expensive, with high resistance to corrosion and oxidation.

To isolate the electrical connection of the wire to the die paddle or thermal pad, a non-conductive die attach film (DAF) is suggested. A DAF material is mainly composed of polymers, resins and silica fillers and it is known in semiconductor industry as an alternative to semiconductor glue in bonding the semiconductor die to the thermal pad. The resins in this material are the adhesion promoter of the DAF where it adheres from the

backside of the backside of the metallized silicon die and die paddle. On the other hand, the polymer and silica fillers are the non-conductive foundation of the DAF providing a specified distance between conductive pad and die paddle.

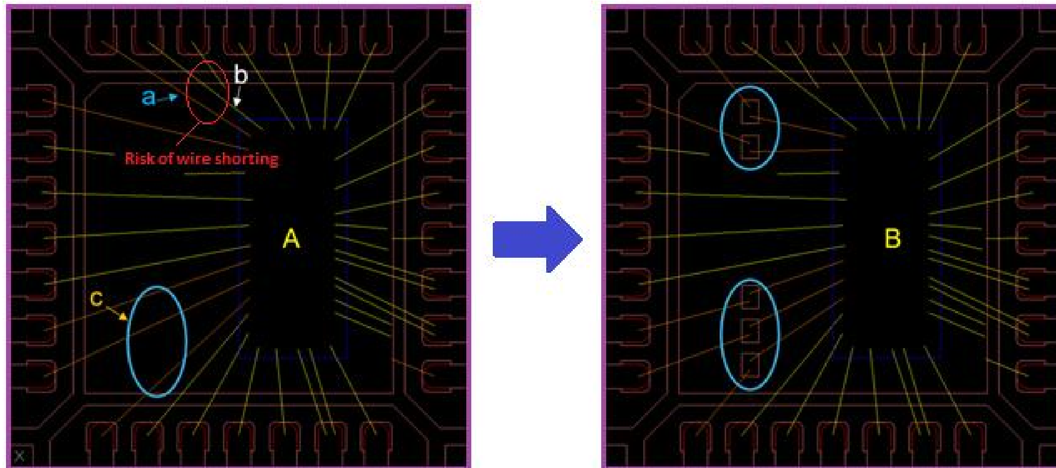

Fig. 1. Package design layout

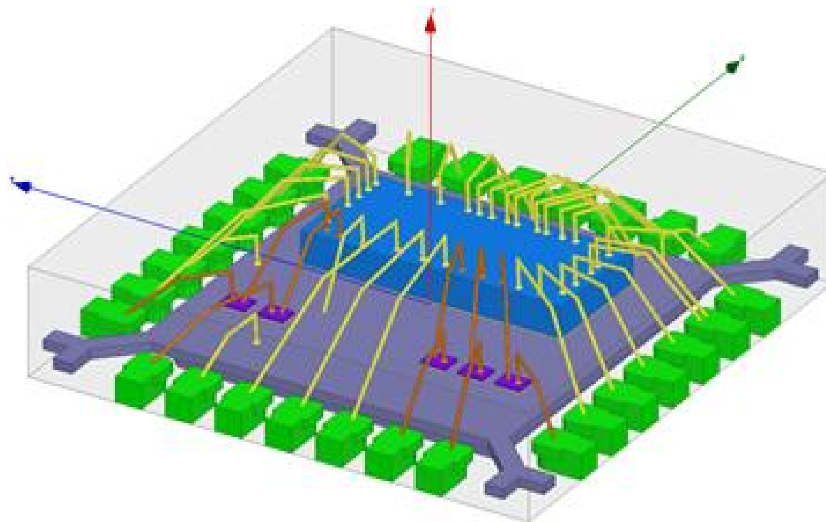

Fig. 2. Package 3D model

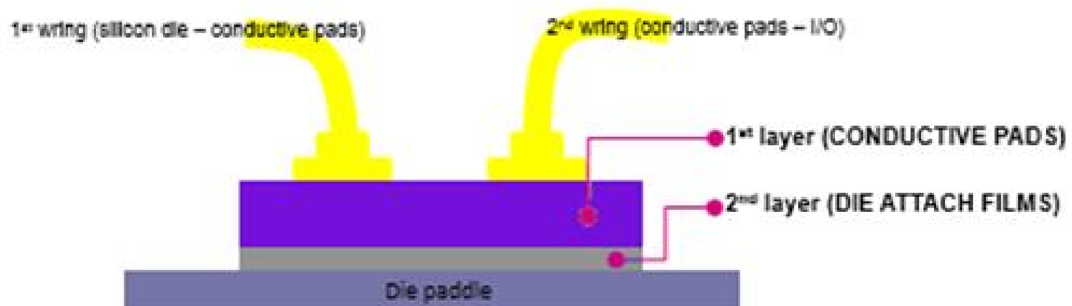

Fig. 3. Metallized silicon die

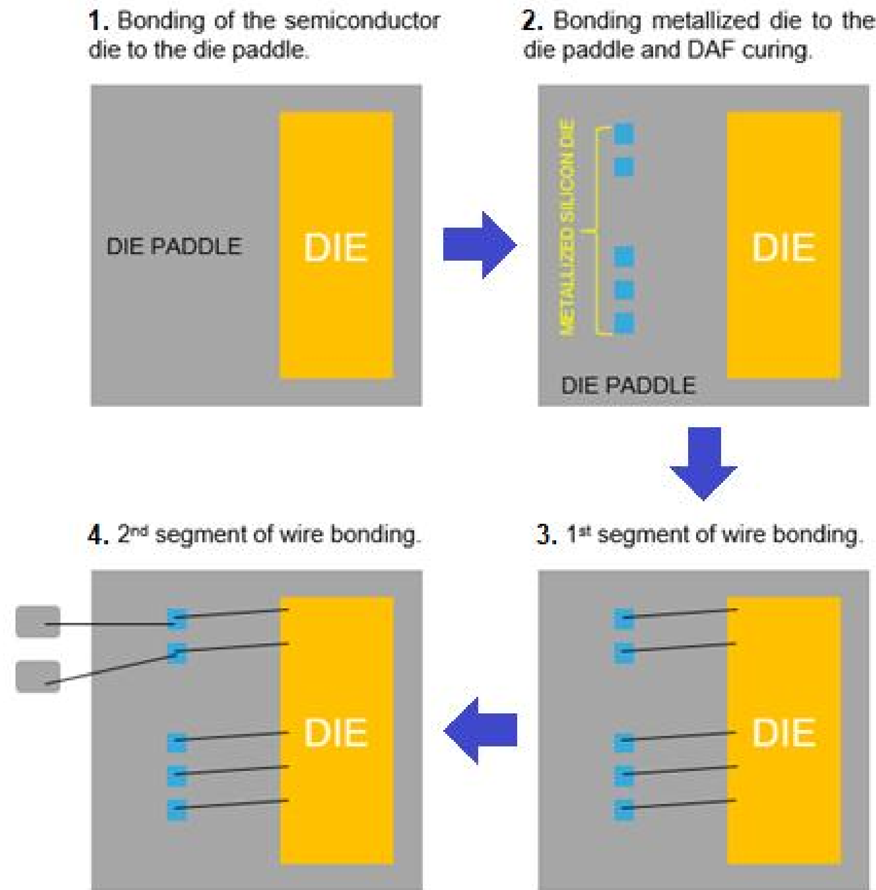

Fig. 4. Assembly flow

Implementing the metallized silicon die in the design, the combined height of the metallized die and DAF should be 40% – 50% of the total height of the semiconductor die. The existing DAF material ranges from 10 – 30 microns thickness and common thickness of the metallized silicon die ranges from 150 – 300 microns.

The method of incorporating the metallized silicon die in the conventional assembly flow of QFN and BGA is illustrated in Fig. 4. Worthy to note assembly process flow varies with the product and the technology [2,6-8]. The metallized silicon die is placed on the die paddle through thermo-compression bonding. This technique uses temperature from the glass below the glass transition state of the DAF material to form partially attach the metallized silicon die to the die paddle. The curing process is required to completely cure the DAF material after it is placed correctly on the thermal pad. The wiring connection is divided into two segments of wire bonding – the 1st wiring is between the silicon die and conductive pads; and the 2nd wiring connection is on the conductive pads and defined I/O pins.

3. CONCLUSION AND RECOMMENDATIONS

Incorporating the use of metallized silicon die applies to large QFN and BGA packages that may require long wire connection. The package design would also prevent long wirebond connection that may sag or be swept during molding process. The solution could be used in succeeding package designs with similar requirement.

Prototypes are helpful for future works to validate the effectiveness of the metallized die design for long wire interconnection on semiconductor QFN and BGA devices. A comparison of this design solution should also be made with other works in the same field. Discussions and

learnings shared in [9-11] are helpful to improve the assembly processes particularly the wirebonding process. Though the paper focused on the long wire requirement, continuous process and design improvement is important to foster and sustain high quality performance of semiconductor products and its assembly manufacturing.

ACKNOWLEDGEMENT

The authors would like to thank the New Product Development & Introduction (NPD-I) colleagues and the Management Team for the utmost support.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan; 2002.
2. Harper C. Electronic packaging and interconnection handbook. 4th ed., McGraw-Hill Education, USA; 2004.
3. Krishnan P, Leong YK, Rafzanjani F, Batumalay N. Die attach film (DAF) for breakthrough in manufacturing (BIM) application. 36th International Electronics Manufacturing Technology Conference, Malaysia; 2014.
4. STMicroelectronics. Assembly and EWS design rules for wire bond Interconnect dice. rev. 54.0; 2019.
5. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.
6. Coombs C, Holden H. Printed circuits handbook. 7th ed., McGraw-Hill Education, USA; 2016.
7. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st Ed., Wiley-IEEE Press, USA; 2006.
8. Nenni D, McLellan P. Fabless: the transformation of the semiconductor industry. CreateSpace Independent Publishing Platform, USA; 2014.
9. Moreno A, Graycochea Jr. E, Gomez FR. Wire shorting elimination through wirebond process optimization of semiconductor sensor device. Journal of Engineering Research and Reports. 2020;13(4):10-14.
10. Tan CE, Liong JY, Dimatira J, Tan J, Kok LW. Challenges of ultimate ultra-fine pitch process with gold wire & copper wire in QFN packages. 36th International Electronics Manufacturing Technology Conference, Malaysia; 2014.
11. Sumagpang Jr. A, Graycochea Jr. E, Gomez FR. Package design improvement for wire shorting resolution. Journal of Engineering Research and Reports. 2020;11(2):41-44.

© 2020 Gomez and Rodriguez; This is an Open Access article distributed under the terms of the Creative Commons Attribution License (http://creativecommons.org/licenses/by/4.0), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sdiarticle4.com/review-history/58632